Temperature dependence and dynamic behaviour of full well capacity in pinned photodiode CMOS image sensors

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***Abstract*—This study presents an analytical model of the Full Well Capacity (FWC) in Pinned Photodiode (PPD) CMOS image sensors. By introducing the temperature dependence of the PPD pinning voltage, the existing model is extended (with respect to previous works) to take into account the effect of temperature on the FWC. It is shown, with the support of experimental data, that whereas in dark conditions the FWC increases with temperature, a decrease is observed if FWC measurements are performed under illumination. This study also shows that after a light pulse, the charge stored in the PPD drops as the PPD tends toward equilibrium. On the base of these observations, an analytical model of the dynamic behaviour of the FWC in non-continuous illumination conditions is proposed. The model is able to reproduce experimental data over six orders of magnitude of time. Both the static and dynamic models can be useful tools to correctly interpret FWC changes following design variations and to accurately define the operating conditions during device characterizations.**

***Index Terms*—CMOS Image Sensor, CIS, pinned photodiode, PPD, Pinning Voltage, full well capacity, FWC, dynamic behaviour, modeling, analytical modeling, temperature, active pixel sensor, APS, capacitance.**

I. Introduction

DRIVEN by low noise applications, Pinned Photodiode (PPD) [1]–[3] CMOS Image Sensors (CIS) (schematized in Fig. 1a) have recently become the main image sensors technology for both commercial and scientific applications. Despite the technology maturity, the literature on the physics of the PPD is not yet exhaustive and the definition, estimation, modeling and measurement of PPD fundamental parameters remain topical subjects. Figure 2 shows the mean sensor output signal as a function of a normalized integration time measured in different operating conditions. As it can be observed, the saturation level, which corresponds here to the Full Well Capacity (FWC) of the PPD, strongly varies with the photon flux (Φ), with temperature (T) and with the Transfer Gate (TG) biasing voltage applied during charge-integration (V_{LOTG}). The dependence of the FWC on the illumination conditions has been addressed in [4] and later in [5], where FWC variations

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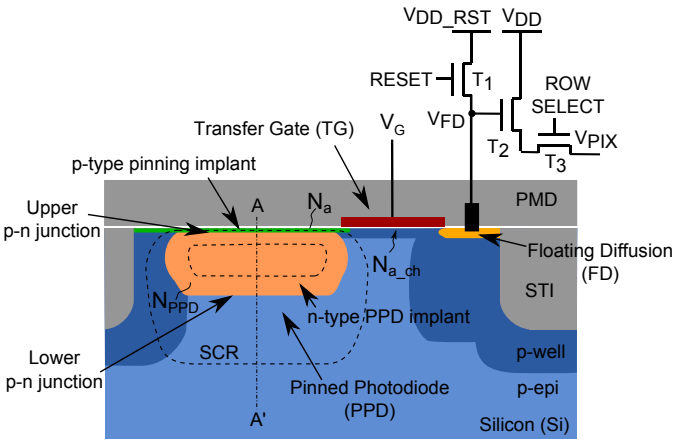
The authors would like to thank CNES and Airbus Defence&Space for supporting the Ph.D of A. Pelamatti, and CNES and CEA for supporting the Ph.D of J.M. Belloir.



(a)

Studied sub-array size	64×128 pixels
Pixel pitch	$7\ \mu$m
PPD size	$2.5\ \mu\mathrm{m} \times 2.5\ \mu\mathrm{m}$
CVF	$20\ \mu\mathrm{V/e^-}$

(b)

Fig. 1. (a) Schematic drawing of the PPD 4 Transistors (4T) Active Pixel Sensor (APS). STI stands for Shallow Trench Isolation, PMD for Pre-Metal Dielectric, SCR stands for Space Charge Region. (b) Details on the device under test.

are explained by means of the TG sub-threshold current. In [6] we recently proposed an analytical model of the FWC, extended to all TG biasing conditions.

In this paper, the analytical model is used as a support to describe the saturation mechanisms responsible for the different FWC levels in the different operating conditions presented in Fig. 2. With respect to [6], the model is extended to take into account the effect of temperature on the FWC. For this purpose, a new temperature model of the pinning voltage is proposed. As it will be discussed, opposite behaviours of the FWC with temperature can be observed depending on the operating conditions. A second contribution of this paper is the extension of the analytical model to non-equilibrium conditions. In particular, this study presents and validates a model of the dynamic behaviour of the FWC following a light pulse.

II. Device under test

The device tested in this study is a 256×256, $7\ \mu$m-pitch pixel array, manufactured in a commercial $0.18\ \mu$m

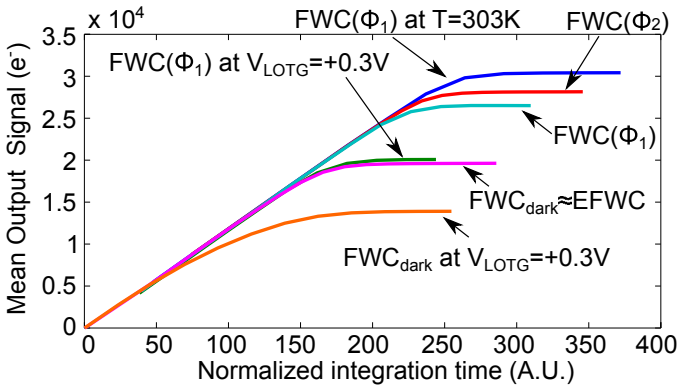


Fig. 2. Mean sensor output signal plotted as a function of a normalized integration time (with respect to the charge generation rate) measured for different operating conditions. $\Phi_1 = 4 \times 10^{13}$ ph/s/cm^2, $\Phi_2 = 2 \times 10^{14}$ ph/s/cm^2. Unless specified, all measurements have been performed at $T = 333$ K and $V_{\mathrm{LOTG}} = -0.5$ V. A.U. stands for Arbitrary Units, EFWC stands for Equilibrium Full Well Capacity (see section V). Details on the device under test can be found in section II.

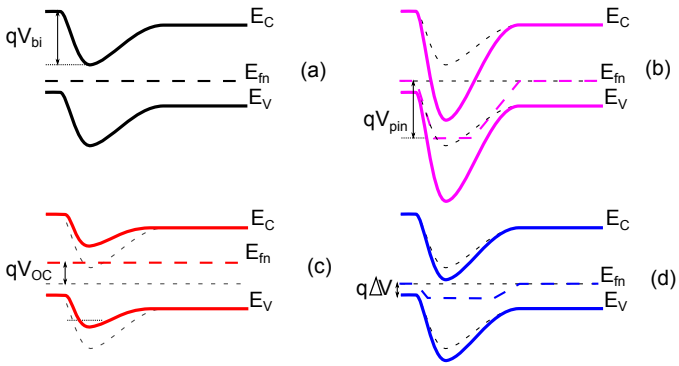


Fig. 3. Schematic of the energy-band diagram of the PPD along the cut A-A' in Fig. 1, (a) at equilibrium, (b) at full depletion (after charge transfer), (c) at full well under illumination (TG in accumulation mode) and (d) at full well in the dark with the TG not in accumualtion mode. The dashed black lines in (b), (c) and (d) represent the band diagram at equilibrium schematized in (a). V_{pin} is the pinning voltage, V_{bi} is the built-in voltage, V_{OC} is the open circuit voltage and $\mathrm{q}\Delta V$ represents the difference between E_{fn} at full well at equilibrium and E_{fn} at full-well considering a leakage of the TG.

PPD CIS process. The pixel array is divided in several sub-arrays of 64×128 pixels, each sub-array having a different PPD/TG design. The measurements presented in this work refer to a sub-array with pixels having a square 2.5×2.5 μm^2 PPD, a long TG and a long Floating Diffusion (FD) (both 2.5 μm wide) on one side. The TG is 0.7 μm long. The Charge to Voltage conversion Factor (CVF) is about 20 μV/e$^-$ (10% standard deviation over the sub-array), which, associated with readout chain characteristics, guarantees that the output voltage saturation is limited by the PPD FWC[1]. Details on the device under test are summarized in Fig. 1b. Measurements are performed within a climatic chamber (with a temperature precision of ± 0.1 K). Unless specified, experimental data correspond to the mean array signal, averaged over 100 acquisitions. The exposure time differs depending on Φ and T.

III. Definition and Estimation of the Full Well Capacity

The FWC corresponds to the maximum amount of charge that can be held by a PPD. It represents a key parameter, as it allows to estimate the dynamic range of the image sensor. If C_{PPD} is the PPD capacitance, the FWC can be expressed as a function of two independent parameters, V_{pin} and V_{OC}:

$$\mathrm{FWC} = \frac{1}{\mathrm{q}} \int_{\mathrm{V_{OC}}}^{\mathrm{Vpin}} \mathrm{C_{PPD}(V_{PPD})}\ \mathrm{dV_{PPD}} \qquad (1)$$

with q the elementary charge.

V_{pin} is the maximum PPD channel potential, often referred to as pinning voltage [7], and is reached during the reset of the photodiode, i.e. during the charge transfer phase in standard PPD CIS operation for a no image lag detector[2]. It corresponds to the maximum variation of the electron quasi-Fermi level E_{fn} at full depletion (Fig. 3b) with respect to equilibrium conditions (Fig. 3a). After the transfer phase, the photodiode potential is floating, and it decreases as charges are integrated in the PPD capacitance. At full well, the total current across the photodiode is null (i.e. the PPD reaches an open circuit condition), therefore, the open circuit voltage V_{OC} in (1) corresponds to the minimum PPD potential. As detailed in the following sections, V_{OC} strongly varies with T, Φ and V_{LOTG}, whereas V_{pin} only depends on T and on technological and geometrical parameters.

IV. Pinning Voltage Temperature Dependence

The pinning voltage, also referred to as pinch-off voltage [8], in analogy to the pinch-off voltage in Junction Field Effect Transistors (JFETs), corresponds to the PPD biasing voltage required to fully deplete the photodiode. It represents a critical design parameter in PPD CIS:

- as shown in (1), the higher is V_{pin}, the higher is the achieved FWC;
- however, V_{pin} must be carefully adjusted, depending on the supply voltage domain, to guarantee a good Charge Transfer Efficiency (CTE) toward the FD [9].

By using an abrupt junction approximation [10], the pinning voltage (V_{pin}) can be expressed as:

$$V_{\mathrm{pin}}(T) \approx \frac{qN_{\mathrm{PPD}}W_{\mathrm{PPD}}^2}{2\epsilon_{\mathrm{Si}}} - V_{\mathrm{bi}}(T) \qquad (2)$$

where ϵ_{Si} is the Si permittivity, W_{PPD} is the depth of buried channel and N_{PPD} is the doping concentrations of the PPD buried channel implant. V_{bi} corresponds to the built-in voltage of the upper junction, which depends on the intrinsic concentration n_{i}, on N_{PPD} and on the pinning implant doping concentration N_{a} [10]. To model the temperature behaviour of V_{bi}, $n_{\mathrm{i}}(T)$ has been modeled as in [11].

To simplify the model in (2) as much as possible, the contribution of the lower p-n junction has been neglected (this

[1]For higher CVF values, the maximum output signal can be limited by the saturation of the readout electronics. In this case, FWC variations do not reflect on the experimental measurements.

[2]If the image sensor presents a non-negligible image lag, the PPD never reaches full depletion, leading to an under-estimation of the FWC and V_{pin}.

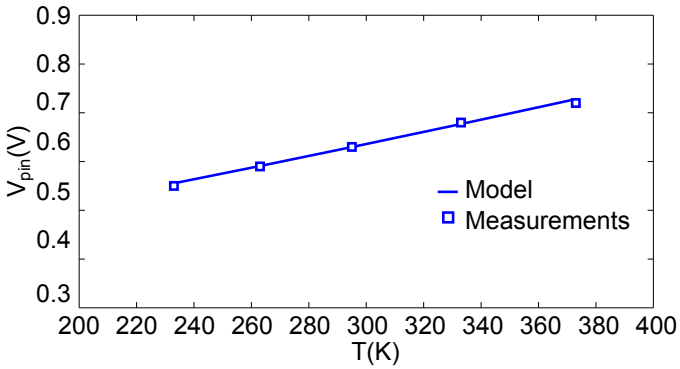


Fig. 4. Pinning voltage as a function of temperature: comparison between experimental data (extracted with the integral method presented in [14]) and the model of (2). The best fit has been obtained for $N_{\mathrm{PPD}} = 2.4 \times 10^{16}$ cm^{-3}, $N_{\mathrm{a}} = 1 \times 10^{18}$ cm^{-3} and $W_{\mathrm{PPD}} = 280$ nm.

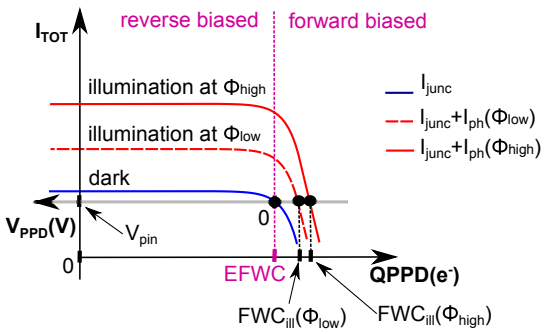


Fig. 5. Schematic of the PPD I-V characteristic in the dark and under two different illumination levels. Full depletion is reached when $Q_{\mathrm{PPD}} = 0$ and $V_{\mathrm{PPD}} = V_{\mathrm{pin}}$. Full well is reached at open circuit condition ($I_{\mathrm{TOT}} = 0$). The open circuit PPD potential V_{OC} (and the corresponding FWC) varies depending on the illumination condition. In particular, EFWC corresponds to the FWC in the dark, whereas $\mathrm{FWC_{ill}}$ is the FWC under illumination. For clarity purposes, schematics are not to scale.

can be justified by the fact that the doping concentration of the epitaxy is much lower than the one of the p+ implant). Geometrical effects such as the geometrical modulation of V_{pin} described in [12] or additional 3D effects such as the ones presented in [8] have also been neglected. The study of the impact of temperature on the geometrical dependence of V_{pin} is left for future studies.

Different pinning voltage extraction techniques have been proposed in the literature [8], [13], [14]. In this work V_{pin} has been extracted from the pinning voltage characteristic [13] with the integral method proposed by Goiffon *et al.* in [14]. As it can be observed in Fig. 4, V_{pin} increases with temperature, and the model in (2) well reproduces the temperature behaviour observed on experimental data.

V. Temperature Dependence of the FWC at Equilibrium

After the reset of the photodiode, the PPD is empty, and the PPD channel potential is equal to the pinning voltage. If the PPD is reset and left in the dark with the TG accumulated, the PPD capacitance is discharged by the dark current I_{junc}, until reaching a saturation level which corresponds to the equilibrium condition of a p-n junction. The saturation charge obtained in dark conditions and neglecting the TG leakage current is referred to as the EFWC [6], [14]. The open circuit voltage V_{OC} corresponding to the EFWC can be obtained by solving:

$$I_{\mathrm{TOT}} = I_{\mathrm{junct}} = I_{\mathrm{sat}} \left(e^{-\frac{V_{\mathrm{OC}}}{n v_{\mathrm{th}}}} - 1 \right) = 0 \qquad (3)$$

with n the diode non-ideality factor ($1 < n < 2$), $v_{\mathrm{th}} = \frac{kT}{q}$ the thermal voltage, and I_{sat} the saturation current [10]. As in standard p-n junctions, the equilibrium condition expressed in (3) holds for $V_{\mathrm{OC}} = 0$. The EFWC can be calculated with (1) as:

$$\mathrm{EFWC(T)} = \frac{1}{\mathrm{q}} \int_0^{\mathrm{Vpin(T)}} \mathrm{C_{PPD}(V_{PPD})}\ \mathrm{dV_{PPD}}. \qquad (4)$$

The blue solid curve in Fig. 5 represents the PPD current in the dark as function of the PPD voltage V_{PPD} and of the stored charge Q_{PPD}. The EFWC corresponds to the open circuit condition (i.e. $I_{\mathrm{junc}} = 0$).

In practice, in nominal PPD CIS operating conditions, the EFWC cannot be reached, and the FWC measured in the dark with TG accumulated corresponds to a saturation charge which is always slightly lower than the EFWC. This difference is attributed to the fact that the TG will always have a small leakage current (sub-threshold current), whichever the TG biasing voltage during integration. To simplify the development of the model, the small difference between EFWC and $\mathrm{FWC_{dark}}$ is neglected. Charge partition phenomena during the transitions of the TG signal [15] (which can result in an artificial increase of the FWC) will also be neglected in this study. Figure 6 shows the measured EFWC as function of temperature. As it can be observed, the model well reproduces the increase of the EFWC with temperature, which is mainly attributed to the increase in V_{pin}.

Whereas the voltage dependence of C_{PPD} is taken into account to fit experimental data in section VI, for clarity purposes C_{PPD} variations will be neglected in the following equations, and the FWC will be simply expressed as:

$$\mathrm{FWC} = \mathrm{EFWC} - \frac{1}{q} V_{\mathrm{OC}} C_{\mathrm{PPD}}. \qquad (5)$$

Note that when $\mathrm{FWC} > \mathrm{EFWC}$, $V_{\mathrm{OC}} < 0$ and the PPD is forward biased (resulting in blooming phenomena).

VI. Temperature Dependence of the FWC at Pseudo-Equilibrium

When the PPD is illuminated, or when the TG is not accumulated during charge integration, the PPD reaches a different saturation level than the EFWC. In the following subsections, the saturation mechanisms for different operating conditions are detailed. In particular, subsection VI-A discusses the behaviour of the FWC when the TG is accumulated during integration, which is a typical biasing mode used to reduce the dark current [16], [17]. In sections VI-B the FWC is modeled for the case in which the TG is not accumulated during integration to implement an anti-blooming function.

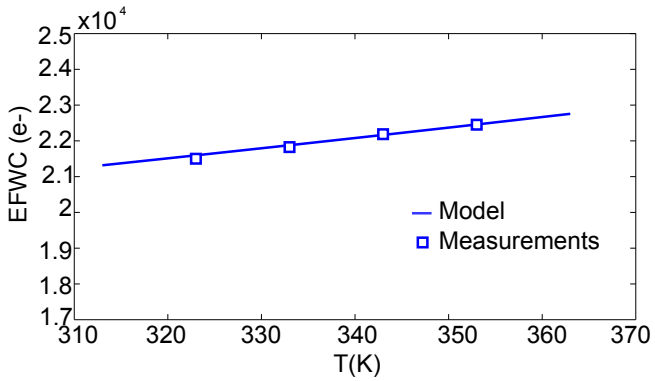


Fig. 6. Measured EFWC as a function of temperature. The best fit has been obtained for $N_{\mathrm{PPD}} = 3.4 \times 10^{16}$ cm^{-3}, $N_{\mathrm{a}} = 1 \times 10^{18}$ cm^{-3} and $W_{\mathrm{PPD}} = 280$ nm.

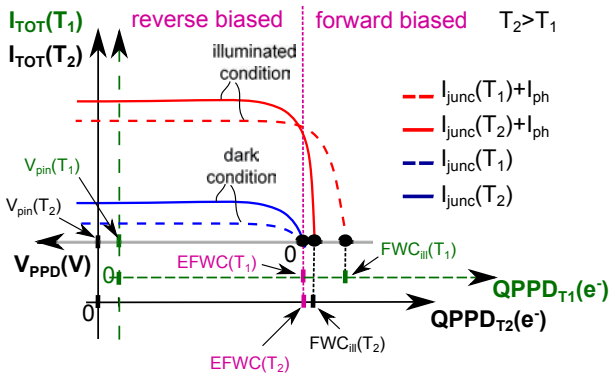


Fig. 7. Schematic of the effect of temperature on the PPD I-V characteristic in the dark and under illumination. For more details on the schematic main features, refer to the explanations in the caption of Fig. 5. The increase in temperature causes an increase in V_{pin} (which is represented as a left shift of the Q_{PPD} axis origin $Q_{\mathrm{PPD}} = 0$), which yields to an increase of the EFWC. As it can be observed, under illumination the FWC tends to decrease as temperature is increased. For clarity purposes, schematics are not to scale.

A. FWC variations as a function of temperature for different illumination conditions (accumulated TG)

If the PPD is exposed to a photon flux Φ, with the TG in accumulation mode, the open circuit condition can be expressed as:

$$I_{\mathrm{sat}}\left(e^{-\frac{V_{\mathrm{OC}}}{nv_{\mathrm{th}}}}-1\right)=I_{\mathrm{ph}}(\Phi) \tag{6}$$

with $I_{\mathrm{ph}}(\Phi)=\eta\Phi$ the photocurrent, where η is the quantum efficiency. The corresponding open circuit voltage can be calculated as:

$$V_{\mathrm{OC}}=-nv_{\mathrm{th}}\ln\left(1+\frac{I_{\mathrm{ph}}(\Phi)}{I_{\mathrm{sat}}}\right). \tag{7}$$

By combining (5) and (7), the FWC can finally be expressed as

$$\mathrm{FWC}(\Phi,T)=\mathrm{EFWC}(T)+\frac{1}{q}C_{\mathrm{PPD}}nv_{\mathrm{th}}\ln\left[1+\frac{I_{\mathrm{ph}}(\Phi)}{I_{\mathrm{sat}}(T)}\right]. \tag{8}$$

As shown in (7), $V_{\mathrm{OC}} < 0$, which means that the PPD is forward biased at full-well (Fig. 3c), and thus FWC>EFWC (which is in agreement with the measurements presented in Fig. 2). Equation (8) shows that the FWC depends logarithmically on the photon flux [4], [6]. This effect is schematized in Fig. 5, where the sum of the dark current and the photocurrent is plotted for two different photon fluxes (solid and dashed red curves). As it can be observed, V_{OC} increases as Φ is increased, which results in a higher FWC.

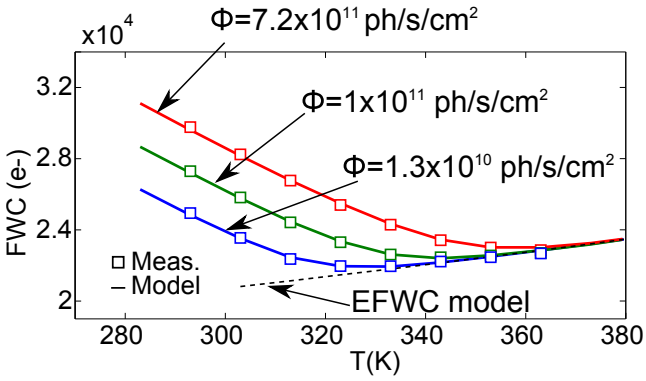


Fig. 8. Full well capacity as a function of temperature measured for 3 different photon fluxes and for the TG in accumulation mode. Square markers represent experimental data, solid lines refer to the FWC modeled as in (8). The dashed line refers to the EFWC modeled as in (4). The best fit has been obtained with the same parameters as in Fig. 6

Equation (8) also indicates that the FWC under illumination is a strong function of temperature. In particular, there are two different and opposite temperature effects, which are schematized in Fig. 7:

- on one hand, as the temperature is increased, there is an increase in the thermal voltage v_{th} and in V_{pin}. These two contributions alone would lead to an increase of the FWC with temperature (as in dark conditions).
- On the other hand, there is an exponential increase in the saturation current I_{sat} [10] which results in a decrease of V_{OC} and in a net decrease of the FWC.

Figure 8 shows the FWC measured for different Φ as a function of temperature. As long as the ratio $\frac{I_{\mathrm{ph}}(\Phi)}{I_{\mathrm{sat}}} >> 1$, the temperature dependence of $I_{\mathrm{sat}}(T)$ is the dominant effect, and the FWC decreases with temperature. If the temperature is increased, the saturation current becomes comparable to the photocurrent and eventually the FWC becomes equal to the EFWC and starts to increase with temperature. As it can be observed, the model can well reproduce the behaviour observed on experimental data.

B. FWC variations as a function of temperature for different TG biasing conditions

Figure 9 shows the FWC measured in the dark plotted as a function of V_{LOTG} for three different measurement temperatures. Three operating regions can be identified:

- for negative V_{LOTG} the FWC corresponds to the EFWC (region A);
- when V_{LOTG} is increased, we observe a transition region (region B) in which the FWC drops moderately with V_{LOTG};
- for even higher V_{LOTG}, the FWC drops linearly with V_{LOTG} (region C).

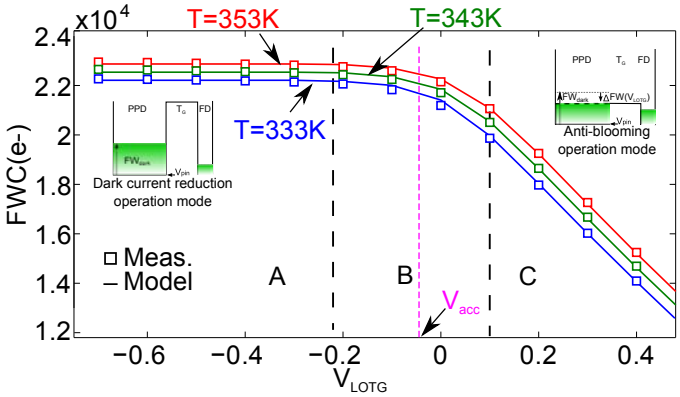


Fig. 9. Measured and simulated FWC as a function of V_{LOTG} at different T in dark conditions. The best fit has been obtained with the same parameters as in Fig. 6.

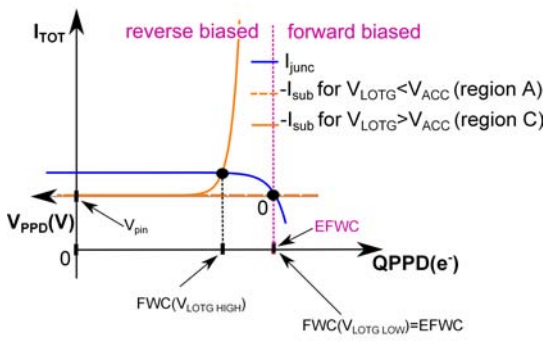


Fig. 10. Schematic of the effect of V_{LOTG} on the PPD I-V characteristic. For clarity purposes, the schematic is not to scale and $-I_{\mathrm{sub}}$ is plotted instead of I_{sub}. Since full well is reached for $I_{\mathrm{junc}} = -I_{\mathrm{sub}}$, the open circuit condition corresponds to the crossing of the two curves.

The knee voltage, indicated in Fig. 9 as V_{acc}, corresponds roughly to the V_{LOTG} at which the TG sub-threshold current (I_{sub}) [10] is comparable to I_{junc}. V_{acc} can also be seen as the biasing voltage V_{LOTG} at which the TG exits the accumulation mode). FWC variations can be modeled by introducing in (3) the contribution of [3] $I_{\mathrm{sub}} = I_{\mathrm{D0}} e^{\frac{V_{\mathrm{LOTG}} - V_{\mathrm{OC}} - V_{\mathrm{T}}}{m v_{\mathrm{th}}(T)}}$:

$$I_{\mathrm{D0}} e^{\frac{V_{\mathrm{LOTG}} - V_{\mathrm{OC}} - V_{\mathrm{T}}}{m v_{\mathrm{th}}(T)}} + I_{\mathrm{sat}} \left(1 - e^{-\frac{V_{\mathrm{OC}}}{n v_{\mathrm{th}}}}\right) = 0 \qquad (9)$$

where I_{D0} depends on the TG geometrical and physical parameters, m is the TG sub-threshold slope ($m > 1$) and V_{T} is the TG threshold voltage (considering body effect).

To highlight the effect of the different parameters, (9) can be expressed as a function of V_{OC}. In particular, as schematized in Fig. 10:

- in region A ($V_{\mathrm{LOTG}} < V_{\mathrm{acc}}$) I_{sub} is negligible with respect to I_{junc}, thus:

$$V_{\mathrm{OC_A}} \approx 0 \qquad (10)$$

- in region C ($V_{\mathrm{LOTG}} > V_{\mathrm{acc}}$) $I_{\mathrm{sub}} >> I_{\mathrm{sat}}$, thus:

$$V_{\mathrm{OC_C}} = V_{\mathrm{LOTG}} - V_{\mathrm{T}} - n v_{\mathrm{th}} \ln\left(\frac{I_{\mathrm{sat}}}{I_{\mathrm{D0}}}\right) \qquad (11)$$

where to simplify the expression it is assumed that $n, m = 1$[4].

Combining (10) and (11) with (5) gives, respectively:

$$\mathrm{FWC}_A(T) = \mathrm{EFWC}(T) \qquad (12)$$

$$\mathrm{FWC}_C(T) = \mathrm{EFWC}(T) - \frac{1}{q} C_{\mathrm{PPD}} \left(V_{\mathrm{LOTG}} - V_{\mathrm{T}}(T)\right) \qquad (13)$$

where the ratio $\frac{I_{\mathrm{sat}}}{I_{\mathrm{D0}}} << 1$ has been neglected. Note that, in region C, the PPD is reversed biased ($V_{\mathrm{OC}} > 0$). In (13) only two parameters can vary with temperature: V_{pin} and V_{T}. As the increase in the FWC with temperature in Fig. 9 is more or less constant at all TG biasing conditions, the increase of V_{pin} can be identified as the dominant effect.

[3]This sub-threshod current contribution can also explain the phenomena reported in [18]

[4]This simplification is not used in the fitting model, where m is calculated as $m = 1 + \frac{1}{C_{\mathrm{ox}}} \sqrt{\frac{\epsilon_{\mathrm{Si}} q N a_{\mathrm{ch}}}{4 \Phi_B}}$ [10] and n is set to 1.75.

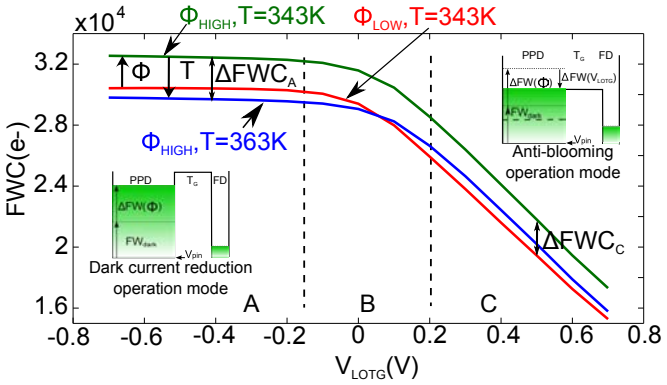


Fig. 11. Full well capacity measured at $T = 343$ K for two photon fluxes ($\Phi_{\mathrm{LOW}} = 3 \times 10^{14}$ ph/s/cm^2 and $\Phi_{\mathrm{HIGH}} = 1.4 \times 10^{15}$ ph/s/cm^2) and at $T = 363$ K for Φ_{HIGH}, as a function of V_{LOTG}.

The reasoning in section VI-B can be extended to the illumination conditions by adding a constant photocurrent to (9). Figure 11 shows the FWC measured for two different photon fluxes and two different temperatures as a function of V_{LOTG}. If $V_{\mathrm{LOTG}} < V_{\mathrm{acc}}$, the FWC is the same as in (8), whereas when $V_{\mathrm{LOTG}} > V_{\mathrm{acc}}$, the FWC drops linearly with V_{LOTG}. As expected from section VI-A, the FWC increases with Φ and decreases with T. It can also be observed that, as the temperature is increased from $T = 343$ K to $T = 363$ K, the FWC decreases more in region A ($\Delta\mathrm{FWC_A} \approx 2000$ e$^-$) than in region C ($\Delta\mathrm{FWC_C} = 1200$ e$^-$). This can be explained by the fact that the temperature dependence of I_{sat} and I_{D0} is not the same (in particular, for the biasing conditions in Fig. 11, I_{sat} is a stronger function of temperature than I_{D0}).

VII. Dynamic Behaviour of the FWC

In the previous sections it has been assumed that, at full well, the PPD is at equilibrium (case of EFWC) or in a pseudo equilibrium state where photo-generation within the SCR is compensated by the charge diffusion toward the p-doped surrounding regions (I_{junc}) and eventually by the leakage of the TG (I_{sub}). However, if the operating conditions are suddenly changed, the time necessary to reach a new pseudo-equilibrium state can be much larger than the time between

two acquisitions. This can lead to measurement uncertainty or to a wrong interpretation of experimental results. In this section, a new analytical model to describe the dynamic behaviour of the FWC in pulsed-light conditions is presented and validated with the support of experimental data. All measurements have been performed at room temperature.

To observe the dynamic evolution of the PPD FWC, a light step has been applied by means of an LED placed at 15 cm from the detector [5], which is operated in rolling shutter mode. The pulse intensity is adjusted to reach the full well condition. The light is first turned ON and 100 images are acquired to ensure that the device has reached pseudo-equilibrium, then the LED is turned OFF. The sequence is repeated, sweeping the integration time from 34 ms (corresponding to the minimum integration time in this configuration) to 60 s. The image acquired during a light step (LED from ON to OFF) is shown in Fig. 12a. The top region (lines 1 to 20) corresponds to the lines which have been read while the LED was still ON. In this region the FWC is equal to the FWC measured under steady illumination (pseudo-equilibrium condition); in the bottom region (line 20 to 40), there is a quick drop in the stored charge. As the device is operated in rolling shutter mode, the FWC drop is attributed to the increase in the delay between the light step and the instant at which the line is readout.

Figure 12b shows the FWC as a function of the time delay between the light step and the line acquisition. The time resolution is 135 μs, which corresponds to the time between the acquisition of two successive lines. As the time delay is increased, the FWC tends asymptotically toward a FWC of about 21 ke- which is close to the EFWC that can be extrapolated at room temperature in Fig. 6. Therefore, applying a light pulse can be a useful technique to fill the PPD to estimate the EFWC at room temperature (and below). Note that an integration time of several tens of seconds must be used to avoid an overestimation of the EFWC. Nevertheless, this integration time is shorter than the time required to fill the PPD only with thermally generated charges (which is a typical method to estimate EFWC).

In order to model the charge transient in the PPD, the data in Fig. 12 has been converted from electrons to PPD voltage, which at saturation corresponds to the open circuit voltage V_{OC}. To simplify the model as much as possible, C_{PPD} variations with V_{OC} are neglected. Under these assumptions, V_{OC} can be approximated to:

$$V_{\mathrm{OC}}(t) \approx \frac{q}{C_{\mathrm{PPD}}} \left[\mathrm{EFWC} - \mathrm{FWC}(t)\right] \tag{14}$$

where $V_{\mathrm{OC}} > 0$ (the PPD is forward biased). Figure 13 shows V_{OC} calculated as (14), plotted as a function of time (in logarithmic scale)[6]. The figure also shows the slope of the curve as a function of time. As it can be observed the slope reaches a first plateau at -0.06 V/decade and then a second plateau at -0.12 V/decade. As discussed in the following, these two different time constants are associated to two different regimes of I_{junc}.

[5]This set-up corresponds to a typical image-lag measurement set-up.

[6]The best fit has been obtained for $C_{\mathrm{PPD}} = 5.4$ fF, which is between the maximum (7.5 fF) and minimum (4 fF) PPD capacitance extracted in [14] for the same pixel geometry at room temperature.

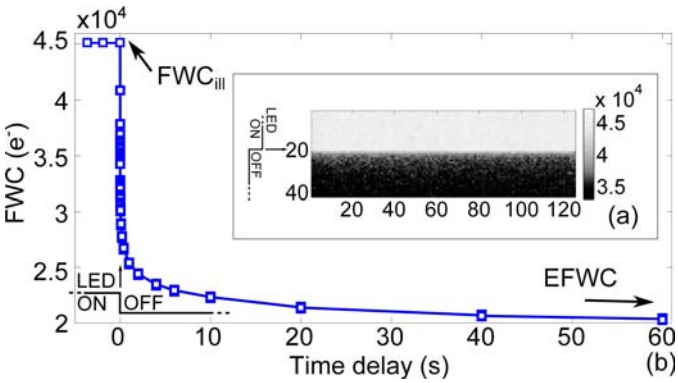


Fig. 12. (a) Image acquired while the light is turned from ON to OFF. A sudden drop in the FWC can be observed after line 20, which corresponds to the last line to be readout before the LED is turned off. (b) Measured mean output charge as a function of the time delay between the light step and the line acquisition at $T = 300$ K and $V_{\mathrm{LOTG}} = -0.5$ V.

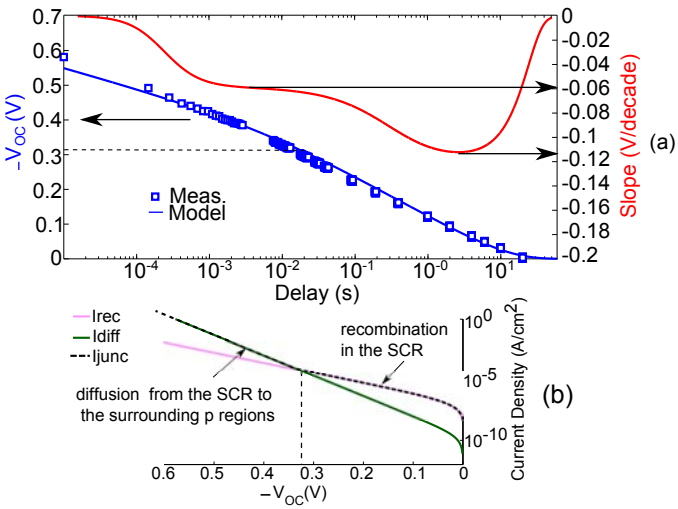


Fig. 13. Measured and simulated V_{OC} as a function of the delay between the light step and the line acquisition. Two regimes corresponding to two different time constants can be identified by observing the slope of $V_{\mathrm{OC}}(t)$. These regimes are attributed to the diffusion of charges from the PPD SCR to the surrounding p-regions and to charge recombination within the SCR, respectively. (b) Simulated diffusion and recombination currents as a function of V_{OC}.

When the light is turned OFF, the time variation of the charge stored in the PPD can be expressed as:

$$\frac{\partial \mathrm{FWC}(t)}{\partial t} = -\frac{1}{q}\left(I_{\mathrm{junc}} + I_{\mathrm{sub}}\right). \tag{15}$$

To simplify the analysis, I_{sub} will be neglected (for consistency, experimental data have been obtained with $V_{\mathrm{LOTG}} = -0.5$ V).

In forward bias, the diode current I_{junc} can be expressed as the sum of two current contributions [10]:

$$I_{\mathrm{rec}} = A_{\mathrm{PPD}} \frac{q n_i W}{2\tau_0} \left[e^{\frac{-qV_{OC}}{2kT}} - 1\right] \tag{16}$$

$$I_{\mathrm{diff}} = A_{\mathrm{PPD}} \frac{q D_n n_i^2}{N_a L_n} \left[e^{\frac{-qV_{OC}}{kT}} - 1\right] \tag{17}$$

where $I_{\rm rec}$ is the recombination current within the SCR, with τ_0 the minority carrier life-time and $I_{\rm diff}$ the diffusion current from the PPD to the surrounding p-regions. As shown in Fig. 13b, the diffusion current dominates at large forward bias, and is responsible for the quick FWC drop following the light pulse. At lower forward voltages the recombination current becomes the main current contribution, which is responsible for the slow descend of the FWC toward the EFWC. The behaviour of the FWC as function of time can be obtained from (14) with

$$V_{\rm OC}(t) = V_{\rm OC}(t_{0^-}) + \frac{1}{C_{\rm PPD}} \int_0^{T_{int}} I_{\rm junc}(t)\ {\rm d}t \qquad (18)$$

where $V_{\rm OC}(t_{0^-})$ is the open circuit voltage corresponding to the FWC with the LED ON ($V_{\rm OC}(t_{0^-}) < 0$). As shown in Fig. 13 the model is able to reproduce the dynamic behavior of the FWC over 6 time delay decades. The small difference at very short delays can be explained by a very fast increase in $C_{\rm PPD}$ at high forward biasing voltages (which is not taken into account in the model).

VIII. Summary and Conclusion

The analytical model of the PPD FWC proposed in [6] has been extended. It has been shown that the FWC is highly dependent on the operating conditions. In particular, the FWC has been studied in three saturation conditions:

- at equilibrium: the FWC corresponds to the EFWC. It only depends on $V_{\rm pin}$ and $C_{\rm PPD}$;
- under illumination with the TG accumulated: the PPD is forward biased, and FWC $>$ EFWC;
- with the TG not accumulated ($V_{\rm LOTG} > V_{\rm acc}$): the PPD is forward biased (FWC $>$ EFWC) or reverse biased (FWC $<$ EFWC) depending on the illumination level.

The model has been validated with the support of experimental data and its range of application has been extended by introducing the effect of temperature on the saturation level. For this purpose, a temperature model of the pinning voltage has been proposed. This study showed that opposite trends can be observed depending on the operating conditions:

- in the dark: the FWC increases for increasing temperature. Its variation is attributed to the increase of $V_{\rm pin}$.
- Under illumination: the FWC decreases for increasing temperatures (as long as $\frac{I_{\rm ph}(\Phi)}{I_{\rm sat}} >> 1$). Its variation is attributed to the exponential increase of $I_{\rm sat}$ with temperature, which results in a lower $V_{\rm OC}$.

Understanding the effect of temperature can be of great importance as it can highlight the variation of one specific parameter (such as the dark current, the pinning voltage or the TG threshold voltage and leakage current) following geometrical variations or radiation campaigns [19].

This work also discussed the dynamic behaviour of the FWC in non steady-state light conditions. It has been shown that once the light source is removed, the FWC drops toward the EFWC as the PPD recovers from forward bias to equilibrium. To explain this behaviour, this study proposed a dynamic model of the FWC based on the different current regimes in a p-n junction. The model is able to reproduce the experimental behaviour over a wide range of time delays (about 6 decades). As the FWC strongly depends on the previous and next operating conditions and on the time elapsed since the experimental variation, the proposed model can be a useful tool to study non-equilibrium transients, e.g. PPD voltage variations between two different operating conditions. Furthermore, these results underline the importance of carefully choosing the pulse intensity in image lag measurements. In particular, if the EFWC condition is exceeded during the light pulse, Charge Transfer Efficiency (CTE) measurements can be affected by the FWC transient toward the EFWC, leading to a wrong interpretation of the experimental results.

Finally, this study not only validates and extends the model proposed in [6], but also validates the pinning voltage extraction method presented in [14] and underlines the importance of relevant FWC levels such as the EFWC in the understanding of the PPD static and dynamic behaviour.

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